Clock generator circuit.

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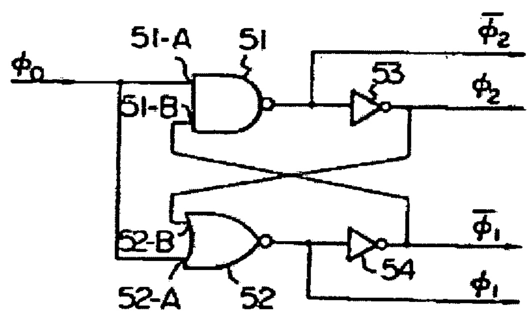
A clock generator circuit for generating two pairs of clock signals comprises a NAND circuit and a NOR circuit cross-coupled to each other and each having an input for receiving a reference clock signal (phi 0). A first inverter is provided between the output of the NAND circuit and the other input of the NOR circuit, and a second inverter is provided between the output of the NOR circuit and the other input of the NAND circuit. A pair of clock signals (phi 2, phi 2) are generated from the NAND circuit and the first inverter, while another pair of clock signals (phi 1, phi 1) are generated from the NOR circuit and the second inverter.

Fig. 5



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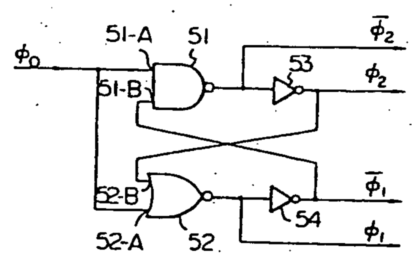
(54) **Clock generator circuit.**

(57) A clock generator circuit for generating two pairs of clock signals (ϕ_2, $\bar{\phi}_2$ - ϕ_1, $\bar{\phi}_1$) comprises a NAND circuit (51) and a NOR circuit (52) cross-coupled to each other and each having an input for receiving a reference clock signal (ϕ_0). A first inverter (53) is provided between the output of the NAND cicuit (51) and the other input of the NOR circuit (52), and a second inverter (54) is provided between the output of the NOR circuit (52) and the other input of the NAND circuit (51). A pair of clock signals ($\bar{\phi}_2$, ϕ_2) are generated from the NAND circuit (51) and the first inverter (53), while the other pair of clock signals (ϕ_1, $\bar{\phi}_1$) are generated from the NOR circuit (52) and the second inverter (54). Unwanted overlap of such clock signals can thereby be avoided.

Fig. 5



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CLOCK GENERATOR CIRCUIT

The present invention relates to a clock generator circuit for generating two pairs of clock signals by using a reference clock signal.

As the case may require, four clock signals, that is, two pairs of clock signals are used. For example, such clock signals are used in a switched capacitor integrator. In this case, it is necessary that a pair of clock signals opposite in phase to each other are not overlapped with another pair of clock signals opposite in phase to each other.

One conventional clock generator circuit comprises a pair of NOR circuits cross-coupled to each other, which serve as an R-S flip-flop. This clock generator circuit generates two non-overlapping clock signals ϕ_1 and ϕ_2 opposite in phase to each other. (See: Electronics, page 99, January 20, 1977.) In this circuit, when an inverter is connected to the output terminal of each of the NOR circuits, two inverted clock signals $\bar{\phi}_1$ and $\bar{\phi}_2$ of the clock signals ϕ_1 and ϕ_2 are also obtained. Thus, the clock generator circuit associated with such inverters generates two pairs of clock signals ϕ_1 and $\bar{\phi}_1$, and ϕ_2 and $\bar{\phi}_2$.

However, in the above-mentioned circuit, due to fluctuation in manufacture, the delay time of each of the inverters is fluctuated. At worst, this delay time is so long that the clock signal $\bar{\phi}_1$ may be overlapped with the clock signals ϕ_2 and $\bar{\phi}_2$ and in addition, the clock signal $\bar{\phi}_2$ may be overlapped with the clock signal ϕ_1 and $\bar{\phi}_1$.

It is desirable to reduce the likelihood of such overlap occurring.

According to the present invention, there is provided a clock generator circuit for generating two pairs of clock signals by using a reference clock signal, comprising:

first and second logic circuits, each having first and second input terminals and an output terminal, for generating first and second clock signals, respectively, the first input terminal of each of the first and second logic circuits receiving the reference clock signal; a first delay circuit, connected between the output terminal of the first logic circuit and the the second input terminal of the second logic circuit, for delaying and inverting the first clock signal so as to generate a third clock signal which forms a pair with the first clock signal; a second delay circuit, connected between the output terminal of the second logic circuit and the second input terminal of the first logic circuit, for delaying and inverting the second clock signal so as to generate a fourth clock signal which forms a pair with the second clock signal; the first logic circuit detecting a change of the potential of the fourth clock signal so as to change the potential of the first clock signal, when the potential of the reference clock signal is high; and the second logic circuit detecting a change of the potential of the third clock signal so as to change the potential of the second clock signal, when the potential of the reference clock is low.

The present invention will be more clearly understood from the description as set forth below contrasting the present invention with the conventional circuit and with reference to the accompanying drawings, wherein:

Fig. 1 is a circuit diagram illustrating a general switched capacitor integrator;

Figs. 2A through 2D are timing diagrams showing the signals appearing in the circuit of Fig. 1;

Fig. 3 is a logic circuit diagram illustrating one conventional clock generator circuit;

Figs. 4A through 4F are timing diagrams showing the signals appearing in the circuit of Fig. 3;

Fig. 5 is a logic circuit diagram illustrating an embodiment of the clock generator circuit according to the

present invention;

Figs. 6A through 6E are timing diagrams showing the signals appearing in the circuit of Fig. 5;

Fig. 7 is a logic circuit diagram illustrating another embodiment of the clock generator circuit according to the present invention; and

Figs. 8A through 8G are timing diagrams showing the signals appearing in the circuit of Fig. 7.

In Fig. 1, which illustrates a general switched capacitor integrator, SW_1 and SW_2 are switches; C_1 and C_2 are capacitors; and OP is an operational amplifier. In this case, the capacitor C_2 forms a negative feedback path of the operational amplifier OP. When the switch SW_1 is turned on, the capacitor C_1 is charged by an input voltage V_{in}. After that, at the next timing, the switch SW_1 is turned off and, in turn, the switch SW_2 is turned on. As a result, the charges stored in the capacitor C_1 are moved to the capacitor C_2. Since the operational amplifier OP operates so as to hold its input terminal (-) at the ground level, an output voltage V_{out} appears in accordance with the quantity of the charges stored in the capacitor C_1.

The input voltage V_{in} is sampled by repeating the above-mentioned operation at a frequency of, for example, 128 kHz, so that the output voltage V_{out}, corresponding to an integrated value of the sampled voltages, is obtained.

In Fig. 1, each of the switches SW_1 and SW_2 comprises a CMOS (Complementary MOS) circuit formed by a p-channel type transistor and a n-channel type transistor. Therefore, when the potential of a clock signal ϕ_1 and the potential of its inverted signal $\overline{\phi}_1$ are high and low, respectively, the switch SW_1 is turned on, while, when the potential of each of the signals ϕ_1 and $\overline{\phi}_1$ are low and high, respectively, the switch SW_1 is turned off. Similarly, when the potential of a clock signal ϕ_2 and the potential of its inverted signal $\overline{\phi}_2$ are high and low, respectively, the switch SW_2 is turned on, while, when the

potential of each of the signals ϕ_2 and $\overline{\phi}_2$ are low and high, respectively, the switch SW_2 is turned off.

It should be noted that the switches SW_1 and SW_2 should not be simultaneously turned on. If the switches SW_1 and SW_2 are simultaneously turned on, the capacitor C_2 is charged directly by the input voltage V_{in} and as a result, a normal integration operation can not be performed.

Figs. 2A through 2D are timing diagrams showing the signals appearing in the circuit of Fig. 1. As illustrated in Figs. 2A through 2D, in order to prevent the switches SW_1 and SW_2 (Fig. 1) from being turned on simultaneously, a pair of the clock signals ϕ_1 and $\overline{\phi}_1$ are non-overlapped with the other pair of the clock signals ϕ_2 and $\overline{\phi}_2$. In more detail, the high potential of the clock signal ϕ_1 is non-overlapped with the high potential of the clock signal ϕ_2 and the low potential of the clock signal $\overline{\phi}_2$. In addition, the low potential of the clock signal $\overline{\phi}_1$ is non-overlapped with the high potential of the clock signal ϕ_2 and the low potential of the clock signal $\overline{\phi}_2$.

Fig. 3 is a logic circuit diagram illustrating one conventional clock generator circuit. As illustrated in Fig. 3, the clock generator circuit comprises two NOR circuits 31 and 32 cross-coupled to each other which serve as an R-S flip-flop. (See: Electronics, page 99, January 20, 1977.) The NOR circuit 31 receives a reference clock signal ϕ_0 directly, while the NOR circuit 32 receives the reference clock signal ϕ_0 via an inverter 33. Each of the NOR circuits 31 generates clock signals ϕ_1 and ϕ_2, respectively, and in addition, clock signals $\overline{\phi}_1$ and $\overline{\phi}_2$ are obtained by inverting the clock signals ϕ_1 and ϕ_2, respectively. For this purpose, two inverters 34 and 35 are provided. Thus, two pairs of clock signals ϕ_1 and $\overline{\phi}_1$, and ϕ_2 and $\overline{\phi}_2$ are obtained.

Figs. 4A through 4F are timing diagrams showing the signals in the circuit of Fig. 3. Referring to Figs. 4A

through 4F, the operation of the circuit of Fig. 3 will now be explained. At a time t_1, the potential of the reference clock signal ϕ_0 is changed from low to high, as illustrated in Fig. 4A and, in turn, at a time t_2, the potential of a signal $\overline{\phi}_0$ is changed from high to low, as illustrated in Fig. 4B. In this state, since the potential at an input terminal 31-B of the NOR circuit 31, which is the same as the potential of the clock signal ϕ_2 as illustrated in Fig. 4E, remains low, the NOR circuit 31 detects the change of the potential at an input terminal 31-A thereof, so that, at a time t_3, the potential of the clock signal ϕ_1 is changed from high to low, as illustrated in Fig. 4C and, in turn, at a time t_4, the potential of the clock signal $\overline{\phi}_1$ is changed from low to high, as illustrated in Fig. 4D. In addition, in this state, since the potential at an input terminal 32-A of the NOR circuit 32, which is the same as the potential of the signal $\overline{\phi}_0$ as illustrated in Fig. 4B, remains low, the NOR circuit 32 detects the change of the potential at an input terminal 32-B thereof, so that, at a time t_5, the potential of the clock signal ϕ_2 is changed from low to high, as illustrated in Fig. 4E and, in turn, at a time t_6, the potential of the clock signal $\overline{\phi}_2$ is changed from high to low, as illustrated in Fig. 4F.

As illustrated in Figs. 4C, 4E and 4F, the high potential of the clock signal ϕ_1 is never overlapped with the high potential (clock pulse) of the clock signal ϕ_2 and the low potential of the clock signal $\overline{\phi}_2$. Contrary to this, with regard to the clock signal $\overline{\phi}_1$, as illustrated in Figs. 4D, 4E and 4F, if $\tau_1 > \tau_2$ where τ_1 is a delay time of the inverter 34 and τ_2 is a delay time of the NOR circuit 32, the low potential of the clock signal $\overline{\phi}_1$ is overlapped with the high potential of the clock si al ϕ_2. In addition, if $\tau_1 > \tau_2 + \tau_3$ where τ_3 is a delay time of the inverter 35, the low potential $\overline{\phi}_1$ is also overlapped with the low potential of the clock signal $\overline{\phi}_2$.

Similarly, when the potential of the reference clock

signal ϕ_0 is changed from high to low, as illustrated in Figs. 4C, 4D and 4E, the high potential of the clock signal ϕ_2 is never overlapped with the high potential of the clock signal ϕ_1 and the low potential of the clock signal $\bar{\phi}_1$. Contrary to this, with regard to the clock signal $\bar{\phi}_2$, as illustrated in Figs. 4C, 4D and 4F, if $\tau_3 > \tau_4$ where τ_4 is a delay time of the NOR circuit 31, the low potential of the clock signal $\bar{\phi}_2$ is overlapped with the high potential of the clock signal ϕ_1. In addition, if $\tau_3 > \tau_4 + \tau_1$, the low potential of the clock signal $\bar{\phi}_2$ is overlapped with the low potential (clock pulse) of the clock signal $\bar{\phi}_1$.

However, the delay time τ_1 of the inverter circuit 34 and the delay time τ_3 of the inverter 35 are often fluctuated due to fluctuation in manufacture. Accordingly, it may happens that $\tau_1 > \tau_2$ (or $\tau_2 + \tau_3$) or $\tau_3 > \tau_4$ (or $\tau_4 + \tau_1$) is satisfied. Thus, in the circuit of Fig. 3, the clock signals ϕ_1 and $\bar{\phi}_1$ may be overlapped with the clock signals ϕ_2 and $\bar{\phi}_2$.

Fig. 5 is a logic circuit diagram illustrating an embodiment of the clock generator circuit according to the present invention. As illustrated in Fig. 5, the clock generator circuit comprises a NAND circuit 51 and a NOR circuit 52 cross-coupled to each other, and two inverters 53 and 54. A reference clock signal ϕ_0 is supplied commonly to an input terminal 51-A of the NAND circuit 51 and an input terminal 52-A of the NOR circuit 52. The NOR circuit 52 generates a clock signal ϕ_1 and in turn, the inverter 54 generates a clock signal $\bar{\phi}_1$ which forms a pair with the clock signal ϕ_1 , while the NAND circuit 51 generates a clock signal $\bar{\phi}_2$ and in turn, the inverter 53 generates a clock signal ϕ_2 which forms a pair with the clock signal $\bar{\phi}_2$. Thus, two pairs of the clock signals ϕ_1 and $\bar{\phi}_1$, ϕ_2 and $\bar{\phi}_2$ are obtained.

Figs. 6A through 6E are timing diagrams showing the signals appearing in the circuit of Fig. 5. Referring to Figs. 6A through 6E, the operation of the circuit of Fig. 5

will now be explained. At a time t_1, the potential of the reference clock signal ϕ_0 is changed from low to high, as illustrated in Fig. 6A. In this state, since the potential at the input terminal of the NOR circuit 52 remains low, the NOR circuit 52 detects the change of the potential at the input terminal 52-A so that, at a time t_2, the potential of the clock signal ϕ_1 is changed from high to low as illustrated in Fig. 6B and in turn, at a time t_3, the potential of the clock signal $\bar{\phi}_1$ is changed from low to high as illustrated in Fig. 6C. In addition, in this state, since the potential at the input terminal 51-A of the NAND circuit 51, which is the same as the potential of the reference clock signal ϕ_0, remains high as illustrated in Fig. 6A, the NAND circuit 51 detects the change of the potential at the input terminal 51-B so that, at a time t_4, the potential of the clock signal $\bar{\phi}_2$ is changed from high to low as illustrated in Fig. 6E and, in turn, the potential of the clock signal ϕ_2 is changed from low to high as illustrated in Fig. 6D.

As illustrated in Figs. 6B, 6D and 6E, since the rise of the potential of the clock signal ϕ_2 and the fall of the potential of the clock signal $\bar{\phi}_2$ follow the fall of the potential of the clock signal ϕ_1, the high potential of the clock signal ϕ_1 is never overlapped with the high potential of the clock signal ϕ_2 and the low potential of the clock signal $\bar{\phi}_2$. In addition, as illustated in Figs. 6C, 6D and 6E, since the rise of the potential of the clock signal ϕ_2 and the fall of the potential of the clock signal $\bar{\phi}_2$ follow the rise of the potential of the clock signal $\bar{\phi}_1$, the low potential of the clock signal $\bar{\phi}_1$ is never overlapped with the high potential of the clock signal ϕ_2 and the low potential of the clock signal $\bar{\phi}_2$.

On the other hand, at a time t_6, the potential of the reference clock signal ϕ_0 falls as illustrated in Fig. 6A and after that, at a time t_7, the potential of the clock signal $\bar{\phi}_2$ rises as illustrated in Fig. 6E. And, in turn, at a time t_8, the potential of the clock signal ϕ_2 falls

as illustrated in Fig. 6D. After that, at a time t_9, the potential of the clock signal ϕ_1 rises as illustrated in Fig. 6B and, in turn, at a time t_{10}, the potential of the clock signal $\bar{\phi}_1$ falls as illustrated in Fig. 6C. Therefore, the high potential of the clock signal ϕ_2 is never overlapped with the high potential of the clock signal ϕ_1 and the low potential of the clock signal $\bar{\phi}_1$ and, in addition, the low potential of the clock signal $\bar{\phi}_2$ is never overlapped with the high potential of the clock signal ϕ_1 and the low potential of the clock signal $\bar{\phi}_1$.

Fig. 7 is a logic circuit diagram illustrating another embodiment of the clock generator circuit according to the present invention. In Fig. 7, inverters 61 through 68 are added to Fig. 5. The operation of the circuit of Fig. 7 is similar to that of the circuit of Fig. 5.

Figs. 8A through 8G are timing diagrams showing the signals appearing in the circuit of Fig. 7. Referring to Figs. 8A through 8G, the operation of the circuit of Fig. 7 will now be explained. At a time t_1, the potential of the refernece clock signal ϕ_0 rises as illustrated in Fig. 8A. After that, at a time t_2, the potential of a signal ϕ_A generated from the NOR circuit 52 falls, as illustrated in Fig. 8B. As a result, at a time t_3, the potential of the clock signal ϕ_1 falls as illustrated in Fig. 8C and, in turn, at a time t_4, the potential of the clock signal $\bar{\phi}_1$ rises as illustrated in Fig. 8D. After the rise of the clock signal $\bar{\phi}_1$, at a time t_5, the potential of the signal ϕ_B generated from the NAND circuit 51 falls. As a result, at a time t_6, the potential of the clock signal $\bar{\phi}_2$ falls as illustrated in Fig. 8G and, in turn, at a time t_7, the potential of the clock signal ϕ_2 rises as illustrated in Fig. 8F.

As illustrated in Figs. 8D, 8F and 8G, since the rise of the potential of the clock signal ϕ_2 and the fall of the potential of the clock signal $\bar{\phi}_2$ follow the rise of the potential of the clock signal $\bar{\phi}_1$, the low potential of the clock signal $\bar{\phi}_1$ is never overlapped with the high potential

of the clock signal ϕ_2 and the low potential of the clock signal $\bar{\phi}_2$.

In order to prevent the high potential of the clock signal ϕ_1 from being overlapped with the high potential of the clock signal ϕ_2 and the low potential of the clock signal $\bar{\phi}_2$, the following condition should be satisfied:

$$\tau_{11} < \tau_{12} \text{ and } \tau_{11} < \tau_{13} \quad \ldots\ldots (1)$$

where τ_{11} is the total delay time of the inverters 67 and 68; τ_{12} is the total delay time of the inverters 54, 65, 66, the NAND circuit 51 and the inverters 53, 61 and 62; and τ_{13} is the total delay time of the inverters 54, 65, 66, the NAND circuit 51 and the inverters 63 and 64.

On the other hand, at a time t_8, the potential of the reference clock signal ϕ_0 falls as illustrated in Fig. 8A. After that, at a time t_9, the potential of the signal ϕ_B rises as illustrated in Fig. 8E. As a result, at a time t_{10}, the potential of the clock signal $\bar{\phi}_2$ rises as illustrated in Fig. 8G and, in turn, at a time t_{11}, the potential of the clock signal ϕ_2 falls as illustrated in Fig. 8F. After the fall of the potential of the clock signal ϕ_2, at a time t_{12}, the potential of the signal ϕ_A rises as illustrated in Fig. 8B. As a result, at a time t_{13}, the potential of the clock signal ϕ_1 rises as illustrated in Fig. 8C and, in turn, at a time t_{14}, the potential of the clock signal $\bar{\phi}_1$ falls as illustrated in Fig. 8D.

As illustrated in Figs. 8C, 8D and 8F, since the rise of the potential of the clock signal ϕ_1 and the fall of the potential of the clock signal $\bar{\phi}_1$ follow the fall of the potential of the clock signal $\bar{\phi}_2$, the high potential of the clock signal ϕ_2 is never overlapped with the high potential of the clock signal ϕ_1 and the low potential of the clock signal $\bar{\phi}_1$.

In order to prevent the low potential of the clock signal $\bar{\phi}_2$ from being overlapped with the high potential of the clock signal ϕ_1 and the low potential of the clock signal $\bar{\phi}_2$, the following condition should be satisfied:

$$\tau_{14} < \tau_{15} \text{ and } \tau_{14} < \tau_{16} \quad \ldots\ldots (2)$$

where τ_{14} is the total delay of the inverters 63 and 64; τ_{15} is the total delay time of the inverters 53, 61 and 62, the NOR circuit 52 and the inverters 67 and 68; and τ_{16} is the total delay time of the ivnerters 53, 61 and 62, the NOR circuit 52 and the inverters 54, 65 and 66.

Note that the above-mentioned conditions (1) and (2) can be easily attained.

As explained hereinbefore, the clock generator circuit for generating two pairs of clock signals according to the present invention has an advantage in that a pair of clock signals are not overlapped with another pair of clock signals. Therefore, when the clock signals obtained by the clock generator circuit according to the present invention are applied to the switches SW_1 and SW_2 of the switched capacitor integrator of Fig. 1, the switched capacitor integrator can perform a reliable integration operation.

CLAIMS

1. A clock generator circuit for generating two pairs of clock signals by using a reference clock signal, comprising:

first and second logic circuits, each having first and second input terminals and an output terminal, for generating first and second clock signals, respectively, the first input terminal of each of said first and second logic circuits receiving said reference clock signal;

a first delay circuit, connected between the output terminal of said first logic circuit and the second input terminal of said second logic circuit, for delaying and inverting said first clock signal so as to generate a third clock signal which forms a pair with said first clock signal;

a second delay circuit, connected between the output terminal of said second logic circuit and the second input terminal of said first logic circuit, for delaying and inverting said second clock signal so as to generate a fourth clock signal which forms a pair with said second clock signal;

said first logic circuit detecting a change of the potential of said fourth clock signal so as to change the potential of said first clock signal, when the potential of said reference clock signal is high; and

said second logic circuit detecting a change of the potential of said third clock signal so as to change the potential of said second clock signal, when the potential of said reference clock is low.

2. A clock generator circuit as set forth in claim 1, wherein said first and second logic circuits are a NAND circuit and a NOR circuit, respectively.

3. A clock generator circuit as set forth in claim 1, further comprising:

a third delay circuit, connected to the output terminal of said first logic circuit, for delaying

said first clock signal;

a fourth delay circuit, connected to the output terminal of said second logic circuit, for delaying said second clock signal,

the delay time of said third delay circuit being less than the total delay time of said first delay circuit, said second logic circuit and said second delay circuit and being less than the total delay time of said first delay circuit, said second logic circuit and said fourth delay circuit; and

the delay time of said fourth delay circuit being less than the total delay time of said second delay circuit, said first logic circuit and said first delay circuit and being less than the total delay time of said second delay circuit, said first logic circuit and said third delay circuit.

/continued

4. A clock generator circuit comprising:

first and second logic circuits having respective first inputs to which signals derived from a reference clock generator are applied when the generator circuit is in use;

first output circuitry, defining first and second circuit paths arranged to receive a signal output of the said first logic circuit and leading respectively to first and second output points of the generator circuit, for providing at the said first and second output points respectively first and second clock signals, each of which consists of a series of cyclically repeated clock pulses, the second clock signal being substantially the inverse of the first clock signal but being delayed slightly with respect thereto; and

second output circuitry, defining third and fourth circuit paths arranged to receive a signal output of the said second logic circuit and leading respectively to third and fourth output points of the generator circuit, for providing at the said third and fourth output points respectively third and fourth clock signals, each of which consists of a series of cyclically repeated clock pulses which are shorter in duration than the spaces therebetween and are also shorter in duration than the spaces between the clock pulses of each of the said first and second clock signals, the fourth clock signal being substantially the inverse of the third clock signal but being delayed slightly with respect thereto;

characterised in that the said second output point is connected to a second input of the said second logic circuit, and the said fourth output point is connected to a second input of the said first logic circuit, thereby to prevent the clock pulses of the third and fourth clock signals from overlapping in time with the clock pulses of the first and second clock signals.

5. A clock generator circuit as claimed in claim 4, wherein the said fourth clock signal is similar to but substantially 180 degrees out of phase with one of the said first and second clock signals.

6. A clock generator circuit as claimed in claim 4, wherein the said fourth clock signal is similar to but substantially 180 degrees out of phase with the said first clock signal.

Fig. 1

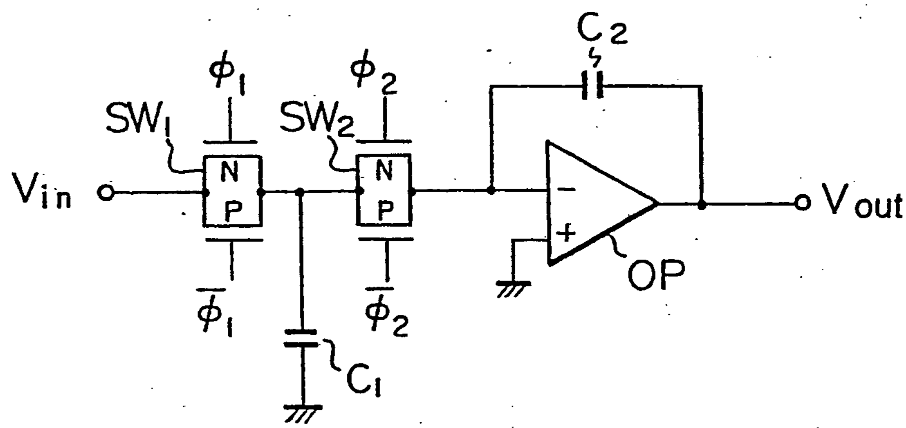
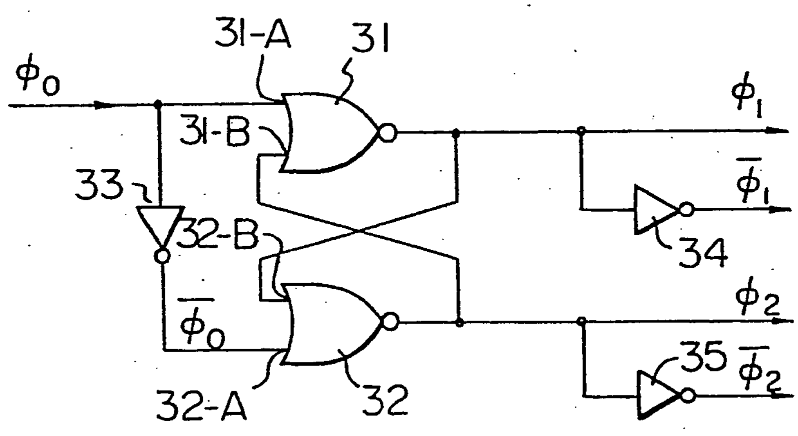

C_2
ϕ_1
ϕ_2
SW_1
SW_2
V_{in}
N
P
N
P
V_{out}
OP
$\overline{\phi}_1$
$\overline{\phi}_2$
C_1

Fig. 3


31-A
31
ϕ_0
31-B
ϕ_1
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32-B
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ϕ_2
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35
$\overline{\phi}_2$
32-A
32

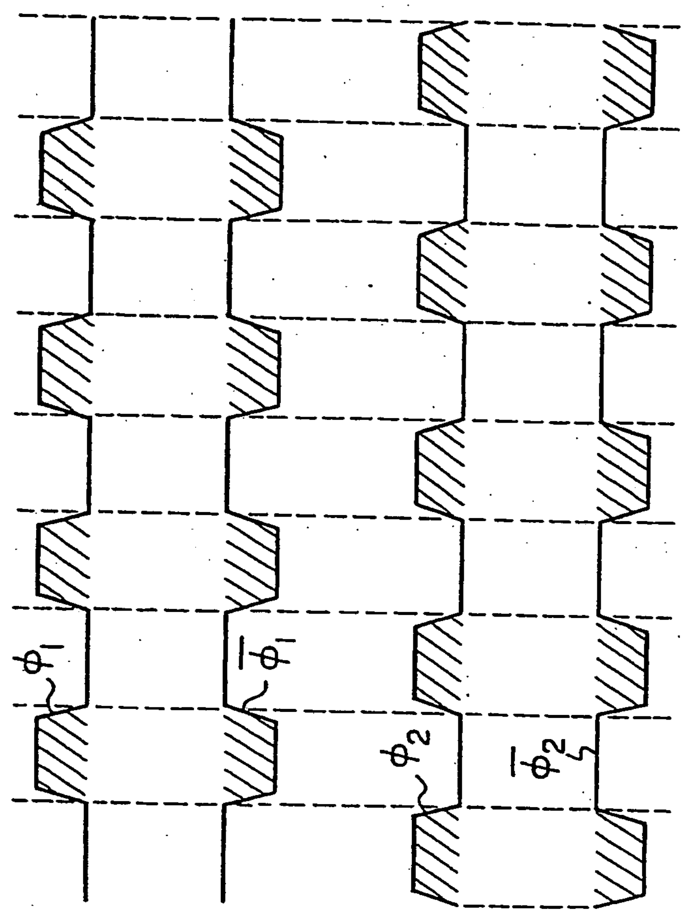


Fig. 2A

Fig. 2B

Fig. 2C

Fig. 2D

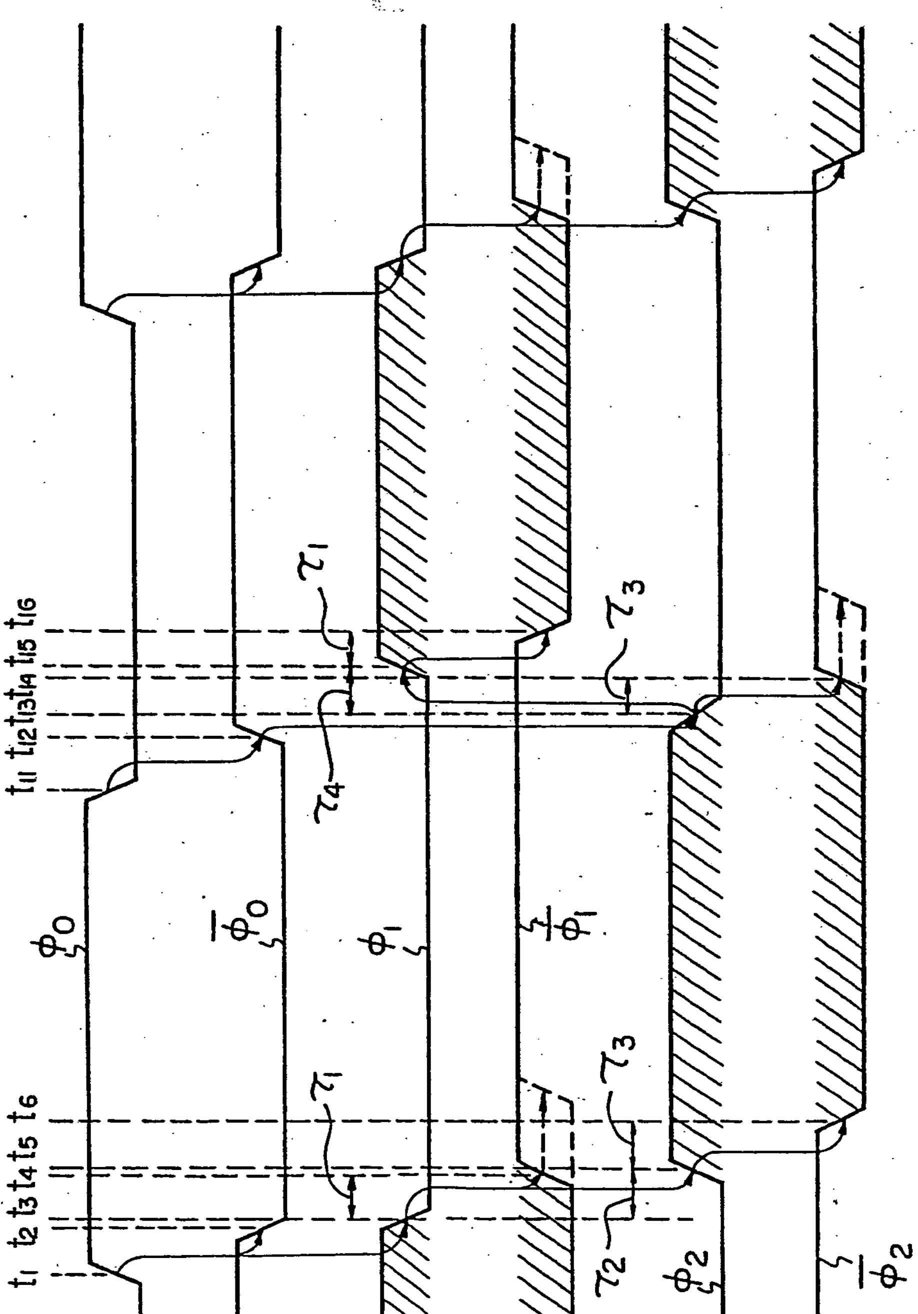


Fig.4A

Fig.4B

Fig.4C

Fig.4D

Fig.4E

Fig.4F

Fig. 5

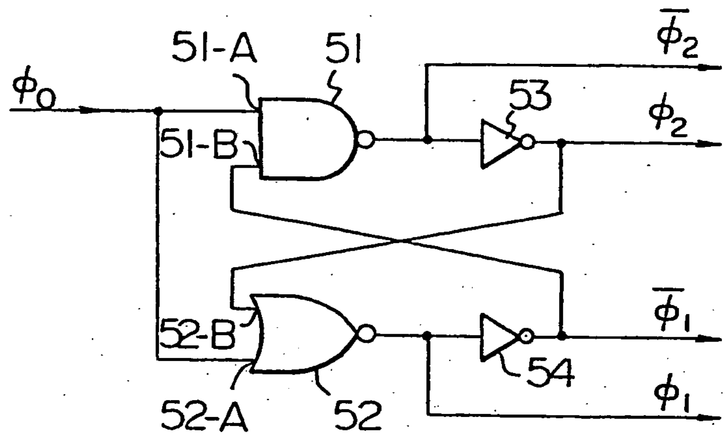
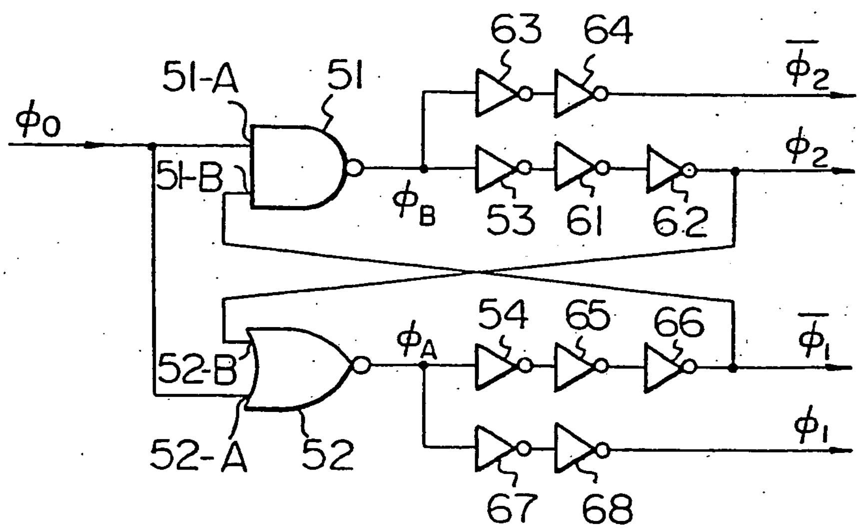

51-A
51
ϕ_0
51-B
53
$\overline{\phi_2}$
ϕ_2
52-B
52-A
52
54
$\overline{\phi_1}$
ϕ_1

Fig. 7


63
64
51-A
51
ϕ_0
51-B
ϕ_B
53
61
62
$\overline{\phi_2}$
ϕ_2
54
65
66
ϕ_A
52-B
52-A
52
$\overline{\phi_1}$
ϕ_1
67
68

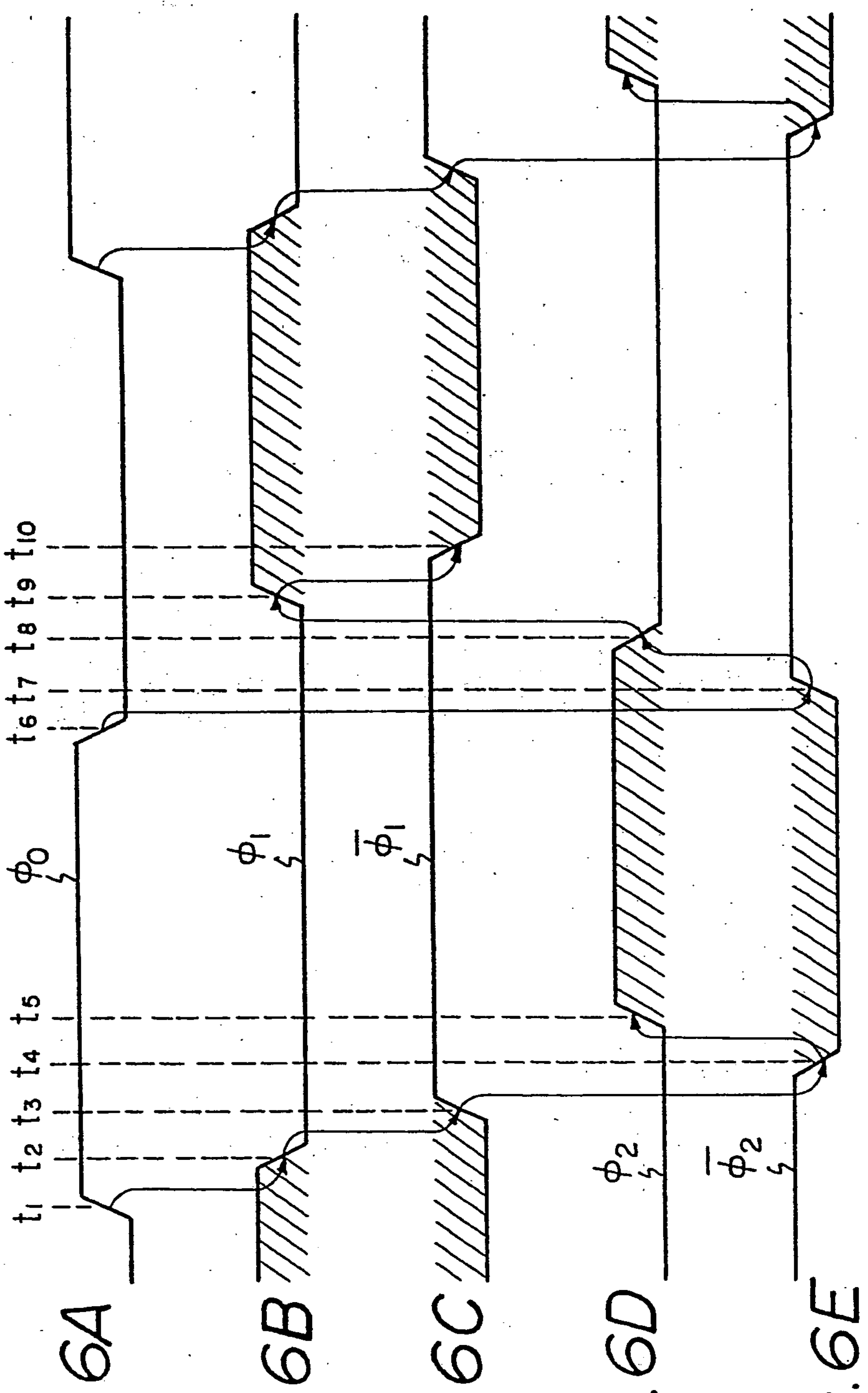


Fig.6A

Fig.6B

Fig.6C

Fig.6D

Fig.6E

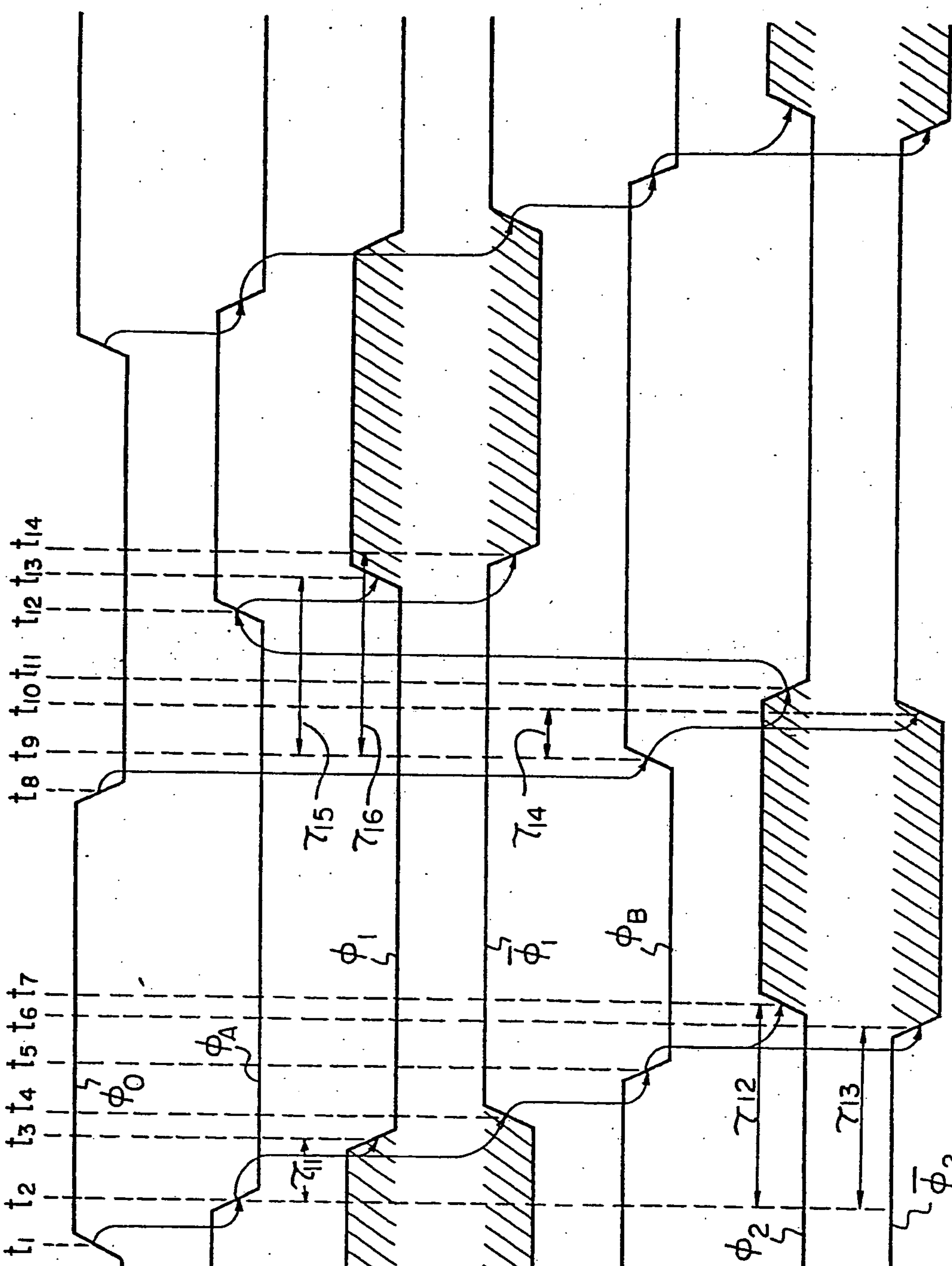


Fig. 8A

Fig. 8B

Fig. 8C

Fig. 8D

Fig. 8E

Fig. 8F

Fig. 8G

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EP 81 30 5484.8

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
Y	US - A - 4 066 919 (R.C. HUNTINGTON) * fig. 8, elements 82, 86; column 7, lines 6 to 32; fig. 8, elements 82, 86, 70, 84, 68, 76, 88, 78; fig. 8, 9 * --	1 4 5,6	H 03 K 5/15
Y	IBM TECHNICAL DISCLOSURE BULLETIN Vol. 20, No. 6, November 1977 F.K. ALLEN "Multiphase Clocking System With Delay Tracking For Control and/or Data Systems" pages 2419 and 2420 * complete article * --	1,4,5,6	TECHNICAL FIELDS SEARCHED (Int.Cl. 3) G 06 F 1/04 H 03 K 3/03 H 03 K 5/15
Y	US - A - 3 961 269 (C.E. ALVAREZ JR) * abstract; fig. 1 and 2; column 3, line 12 to column 4, line 37 * --	1	
Y	US - A - 3 668 436 (S.H. BACON) * abstract; column 1, lines 23 to 40; fig. 2 and 3; column 3, lines 1 to 41 * --	1	CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons
A	FR - A - 2 064 528 (CIE DES COMPTEURS) * fig. 4 and 5 * --	1	
A	FR - A - 2 379 198 (THOMSON-CSF) * fig. 4 * -- ./..	1	
X	The present search report has been drawn up for all claims		&: member of the same patent family, corresponding document

Place of search	Date of completion of the search	Examiner
Berlin	11-02-1982	ARENDT

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A	GB - A - 2 030 403 (SIEMENS AG) * abstract; fig. 1 and 2 * --	1	
A	US - A - 4 140 927 (C.A. FEUCHT) * abstract; fig. 1 and 2 * --	1	
A	ELECTRONIC ENGINEERING, Vol. 50, No. 616 December 1978 S.J. CAHILL "A Single-Chip Two-Phase Clock" pages 27, 29 * complete article * --	1	TECHNICAL FIELDS SEARCHED (Int. Cl.3)
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A	Patent Abstracts of Japan Vol. 2, No. 10, 25 January 1978 page 10409E77 & JP - A - 52 - 127051 -- ./..		

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- page 3 -

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			TECHNICAL FIELDS SEARCHED (Int. Cl.³)